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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,158	09/26/2001	Martin Li	TI-33430	9577

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EXAMINER	
GREY, CHRISTOPHER P	

ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
09/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/964,158	LI ET AL.	
	Examiner	Art Unit	
	Christopher P. Grey	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

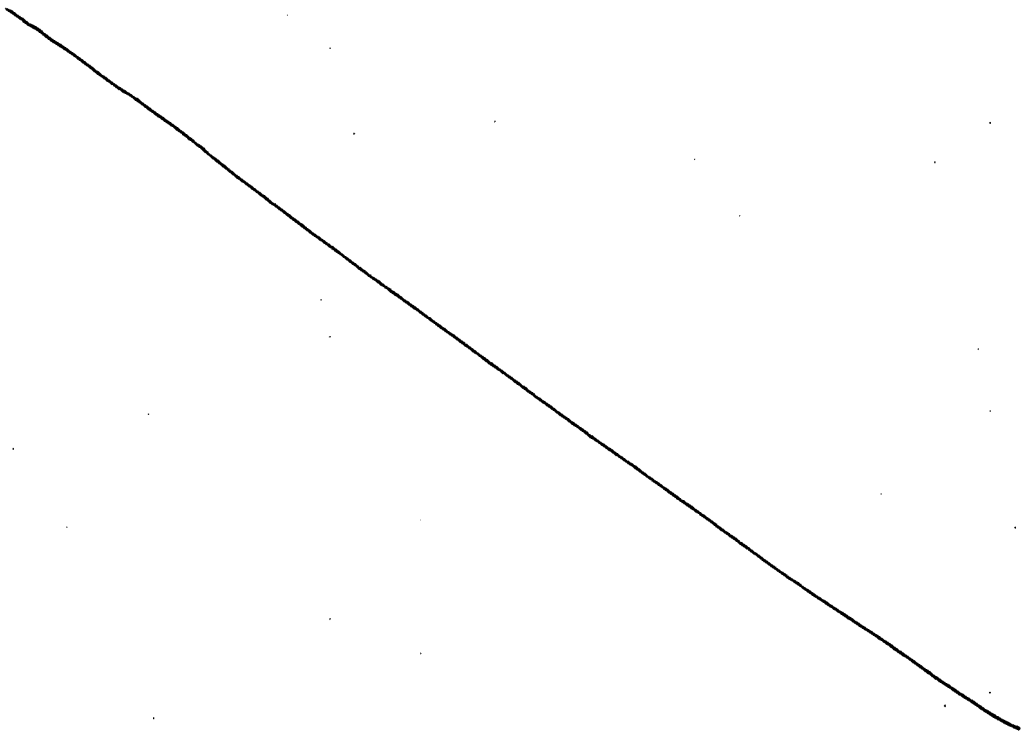
DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1, 10 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims make reference to a 2-stage FIFO, however no where within the specification does it describe or make reference to the FIFO being 2-stage. The specification merely makes reference to the FIFO storing 2 ATM cells, however does not elaborate on why or how the FIFO is 2-stage.



Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7, 10 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider et al. (US 7002979) in view of Jensen (US 6732206).

Claim 1, 10, 14 Schneider discloses an input unit, the input unit receiving data cells.

Schneider discloses an input buffer unit (fig 2, 214, Rx FIFO) receiving data signals and exchangning control signals with the input unit **(fig 2, 200, where the components of the receive subsystem combined form the input unit, where control signals are received and transmitted as shown in fig 3 and Col 6 lines 39-51)**.

Schneider discloses the input unit buffer unit including: a buffer storage unit coupled to the input unit, the buffer storage unit being a two stage, first in/ first out memory unit, the buffer storage unit storing received data cells **(Col 4 lines 30-36)**, the buffer storage unit transferring data cells to the DMA unit in response to a first ready signal **(Col 6 lines 4-14, receiving information that enables transfer of packet data to DMA and fig 2, RX FIFO, 214 and RX DMA 204).**

Schhneider discloses a calculation unit **(Col 5 lines 19-20, checksum calculations).**

Schneider discloses a register (fig 2, 206 and Col 7 lines 55-67), each data cell including a cell portion having an encoded destination location (Col 8 lines 39-41), the calculation unit responsive to the contents of the register and to the cell portion for generating a destination location **(Col 8 lines 29-43, examine layer 3 info including destination address for checksum calculations)** for the data cell in the ATM unit (Col 1 line 60, ATM).

Schneider discloses comparing a field in the data cell with the contents of a register **(Pertaining to claim 10, Col 8 lines 29-37, compares).**

Schneider discloses an output unit (fig 1 elements 102, 104, 108 and 110 make up an interface unit), the output unit including;

An output buffer storage unit, the output buffer unit being a 2 stage FIFO storage unit for storing data cells, the output buffer unit receiving data cells from the DMA unit in response to a second READY signal **(Col 13 lines 26-31, DMA controller controls writing of data from DMA 204, where some form of signal triggers writing, and that signal is equivalent to a ready signal)** with the direct memory access unit **(the network interface 102 has a buffer 1006 in fig 10 for receiving data coming from the DMA 106 in fig 1 and see Col 12 lines 41-64, for FIFO, status data and error signal exchanged)**

Schneider discloses an output unit, the output unit receiving data cells from the output buffer unit and applying data cells to the communication bus, the output unit exchanging control signals with the processing unit (fig 1 depicts the output unit

interfacing a network, where information is exchanged b/w the network and the system disclosed.

Schneider does not specifically disclose and ATM master processing unit. Jensen discloses an ATM master processing unit (fig 1, 10). Jensen also discloses implementing the signals exchanged over the communication bus in UTPOPIA format (Pertaining to claim 14, Col 5 lines 28-35).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the master unit to couple a master unit to the system and network as disclosed by Schneider. The motivation for this combination is for a master to communicate with a group of multi PHYs particularly using UTPOIA **(Col 1 lines 20-29).**

Claim 7 Schneider discloses wherein the ATM slave processing unit includes at least one digital signal CPU **(fig 1 depicts a processor).**

3. Claims 4, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider et al. (US 7002979) in view of Jensen et al. (US 6732206) in further view of Chen et al. (US 5870628)

Claim 4, 11 The combined teachings of Schneider and Jensen disclose a clock domain (Jensen, Col 2 lines 46-65). However the combined teachings do not disclose the buffer storage unit transferring a data cell to the slave data processing unit every clock cycle.

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify that master unit as disclosed by the combined teachings of Schneider and Jensen, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

Claim 12 Schneider does not specifically disclose implementing the signals exchanged over the communcaition bus in UTPOPIA format.

Jensen discloses implementing the signals exchanged over the communication bus in UTPOPIA format (Col 5 lines 28-35).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the master unit to couple a master unit to the system and network as disclosed by Schneider. The motivation for this combination is for a master to communicate with a group of multi PHYs particularly using UTPOIA **(Col 1 lines 20-29).**

4. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider et al. (US 7002979) in view of Jensen et al. (US 6732206) in further view of Kessler et al. (6029212).

Claim 5, 13 The combined teachings of Schneider and Jensen disclose using an address translation unit to determine a destination (Jensen, Col 2 lines 8-24).

However, the combined teachings do not disclose the destination locations being selected from a group of a plurality of central processing units and memory locations, at least one central processing unit and at least one memory location.

Kessler et al. ('Kessler' hereinafter) discloses a translation unit for calculating an address of a memory location, and transferring the data to one (selected) of a multiple number of external registers (Col 2 lines 5-17), where an external register may be equivalent to and comparable to any of a plurality of processing units, a shared memory location or a combination of both..

It would have been obvious to one of the ordinary skill in the art at the time of the invention to specify the result of the translation (destination) as disclosed by the combined teachings, to include external registers, where registers are memory oriented and have several processing functions. The motivation for this specification is to address data to a specific location (Col1 lines12-15).

Response to Arguments

5. Applicant's arguments with respect to claims 1, 10 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600